Course Specification
(Bachelor)

Course Title:	Digital Logic
Course Code:	CNET 233
Program:	Computer & Network Engineering
Department:	Electrical & Electronics Engineering
College:	College of Engineering & Computer Science
Institution:	Jazan University
Version:	14
Last Revision Date:	21 May 2024

Table of Contents

A. General information about the course:

1. Course Identification

1. Credit hours: (3)					
2. Course type					
A.	☐ University	☐ College	☒ Department	☐ Track	☐ Others
B.	☒ Required		☐ Elective		
3. Level/year at which this course is offered: (4th level / 2nd Year)					
4. Course General Description:					
This course presents the various binary systems suitable for representing information in digital systems and binary codes are illustrated. It introduces the basic postulates of Boolean algebra and shows the correlation between Boolean expressions and their corresponding logic diagrams. It covers the map method for simplifying Boolean expressions. The map method is also used to simplify digital circuits constructed with AND-OR, NAND and NOR gates. The procedures to develop and conduct appropriate experimentation for the analysis and design of Combinational and Sequential circuits with Verilog. It deals with various sequential circuit components such as registers, shift registers and counters with memory circuits.					
5. Pre-requirements for this course (if any)**: Nil**					
6. Co-requisites for this course (if any)**: Nil**					
7. Course Main Objective(s):					
• Explain the concept of digital system with various number systems. • Describe the Boolean expressions with Boolean Algebra Theorems. • Simplify the map methods to reduce the Boolean Functions. • Design and simulating of Hardware Description Languages such as Verilog. • Design and apply the applications of Combinational and Sequential circuits. • Analyze and design of Memory elements.					

2. Teaching mode (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	Traditional classroom	60	100%
2	E-learning	-	-
3	Hybrid • Traditional classroom • E-learning	-	-
4	Distance learning	-	-

3. Contact Hours (based on the academic semester)

No	Activity	Contact Hours
1.	**Lectures**	26
2.	**Laboratory/Studio**	26
3.	**Field**	-
4.	**Tutorial**	-
5.	**Others (specify)**	8
Total		60

B. Course Learning Outcomes (CLOs), Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Code of PLOs aligned with the program	Teaching Strategies	Assessment Methods
1.0	**Knowledge and understanding**			
1.1	**Explain** the digital systems and their applications in computer engineering and most current developments.	K3	➢ Lectures ➢ Classroom Discussion	Midterm Exam Final Exam Assignment-1
1.2	**Identify** number systems and their conversion with coding schemes.	K1	➢ Lectures ➢ Classroom Discussion	Midterm Exam Final Exam Assignment-1
1.3	**Describe** Boolean expressions and their simplification using axiomatic properties and K-Map.	K2	➢ Lectures ➢ Classroom Discussion	Midterm Exam Final Exam Assignment-1
2.0	**Skills**			
2.1	**Design** the Boolean function from basic logic gates, universal logic gates and truth tables using latest tools.	S3	➢ Lectures ➢ Classroom Discussion	Midterm Exam Final Exam Assignment-2 Lab Exam
2.2	**Apply** the design of Combinational and Sequential circuit and their use in applications.	S2	➢ Lectures ➢ Classroom Discussion	Final Exam Assignment-2 Mini-Project Lab Exam
2.3	**Analyze** the design with Verilog and working of Registers and their and construction using sequential circuits.	S5	➢ Lectures ➢ Classroom Discussion	Final Exam Mini-Project Assignment-2
2.4	**Communicate** effectively with team members in the group of mini-project	S4	➢ Lectures	Mini-Projects

Code	Course Learning Outcomes	Code of PLOs aligned with the program	Teaching Strategies	Assessment Methods
			➢ Classroom Discussion	
3.0	**Values, autonomy, and responsibility**			
3.1	**Conduct** the projects and experiments with digital circuit kits of combinational and sequential logic and also design them with Verilog.	V1	Lab Exercises	Lab Exam Mini-Project

C. Course Content

No	List of Topics	Contact Hours
1.	**Chapter 1: Digital Systems and Binary Numbers** ● Digital Systems ● History and overview ● Numbers systems and data encoding ● Relevant tools, standards, and/or engineering constraints ● Number-Base Conversions ● Octal and Hexadecimal Numbers ● Complements of Numbers ● Signed Binary Numbers ● Binary Codes – BCD, Gray Codes and ASCII ● Binary Storage and Registers ● Binary Logic and basic logic circuits	5T + 5P
2.	**Chapter 2: Boolean Algebra and Logic Gates** ● Introduction ● Basic Definitions ● Axiomatic Definition of Boolean Algebra ● Basic Theorems and Properties of Boolean Algebra ● Boolean Algebra Applications ● Boolean Functions ● Canonical and Standard Forms ● Other Logic Operations ● Digital Logic Gates – Design of Universal Gates	5T + 5P
3.	**Chapter 3: Gate Level Minimization** ● Introduction ● The Map Method ● Four-Variable K-Map ● Product-of-Sums Simplification ● NAND and NOR Implementation ● Exclusive-OR Function – Parity generator ● Hardware Description Language – Introduction to verilog	5T + 5P
4.	**Chapter 4: Combinational Logic** ● Introduction- Modular design of combinational circuits ● Binary Adder-Subtractor ● Decoders ● Encoders ● Multiplexers ● Verilog Model	3T + 3P
5.	**Chapter 5: Synchronous Sequential Logic** ● Introduction-Modular design of sequential circuits	3T+3P

	• Comparison of combinational and sequential circuits • Storage Elements: Latches • Storage Elements: Flip-Flops • State Equation, State Table and State Diagram of Sequential Circuit.	
6.	**Chapter 6: Registers and Counters** • Registers: Four-bit Register • Shift Registers: Four-bit Shift Register • Serial Transfer and Parallel Transfer • Counters: Definition and Types • Ripple Counters: Binary Ripple Counter • Synchronous Counters • Control and datapath design • Design with programmable logic • System design constraints • Faults models, testing, and design for testability	5T+5P
7.	**Final Exam**	4T+4P
Total		**60**

Self-Study Topics
• Block diagram of Digital Computer • Integrated Circuits and Digital Logic Families • Don't care conditions – K Map • Other Two Level Implementations • Universal Shift Register • Memory and ROM • RAM,ROM,EEPROM and FLASH

D. Students Assessment Activities

No	Assessment Activities *	Assessment timing (in week no)	Percentage of Total Assessment Score
1.	Assignment - 1	5th week	10%
2.	Midterm Exam	7th - 8th week	20%
3	Assignment – 2 / Mini-project	10th week	10%
4.	Lab Exam	13th week	20%
5.	Final Theory Exam	14th week	40%

*Assessment Activities (i.e., Written test, oral test, oral presentation, group project, essay, etc.).

E. Learning Resources and Facilities

1. References and Learning Resources

Essential References	M. Morris Mano and Michael D. Ciletti , " Digital Design with an introduction to HDL, VHDL and System Verilog", Prentice Hall, Pearson Education International, 6th Edition, 2018. ISBN: 9780132774208
Supportive References	Ronald J, Tocci, Neal S. Widmer, and Gregory L. Moss, "Digital Systems: Principles and Applications", Prentice Hall, 10th Edition, 2016.

	ISBN 0-13-111120-5
Electronic Materials	Blackboard: https://lms.jazanu.edu.sa/webapps/blackboard/content/listContentEditable.jsp?content_id=_1197085_1&course_id=_164015_1&mode=reset
Other Learning Materials	--

2. Required Facilities and equipment

Items	Resources
facilities (Classrooms, laboratories, exhibition rooms, simulation rooms, etc.)	One Lecture room equipped with projector.(maximum 30 students at a time)
Technology equipment (projector, smart board, software)	Verilog Simulator – verilator 4.030
Other equipment (depending on the nature of the specialty)	One specialized hardware lab fully equipped with various Hardware Kits Such as Trainer Kit and Experiment Module Kits with Connecting Wires accessories.

F. Assessment of Course Quality

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of teaching	Students	Course Evaluation survey form
Effectiveness of Students assessment	HOD/Committee nominated by HOD	Random re-checking of evaluated answer sheets
Quality of learning resources	Track Leaders	Review meetings and star rating with suggestions for further modification and improvements
The extent to which CLOs have been achieved	Course Teachers and Course Coordinators/QAU Course Coordinators QAU	CLO assessment template that is further verified at course coordinator, Track leader and QAU level.
Other	Students	Course Evaluation survey form

Assessors (Students, Faculty, Program Leaders, Peer Reviewers, Others (specify)

Assessment Methods (Direct, Indirect)

G. Specification Approval

COUNCIL /COMMITTEE	**DEPARTMENT COUNCIL**
REFERENCE NO.	**ENGCSEEE2411**
DATE	**10/10/24**