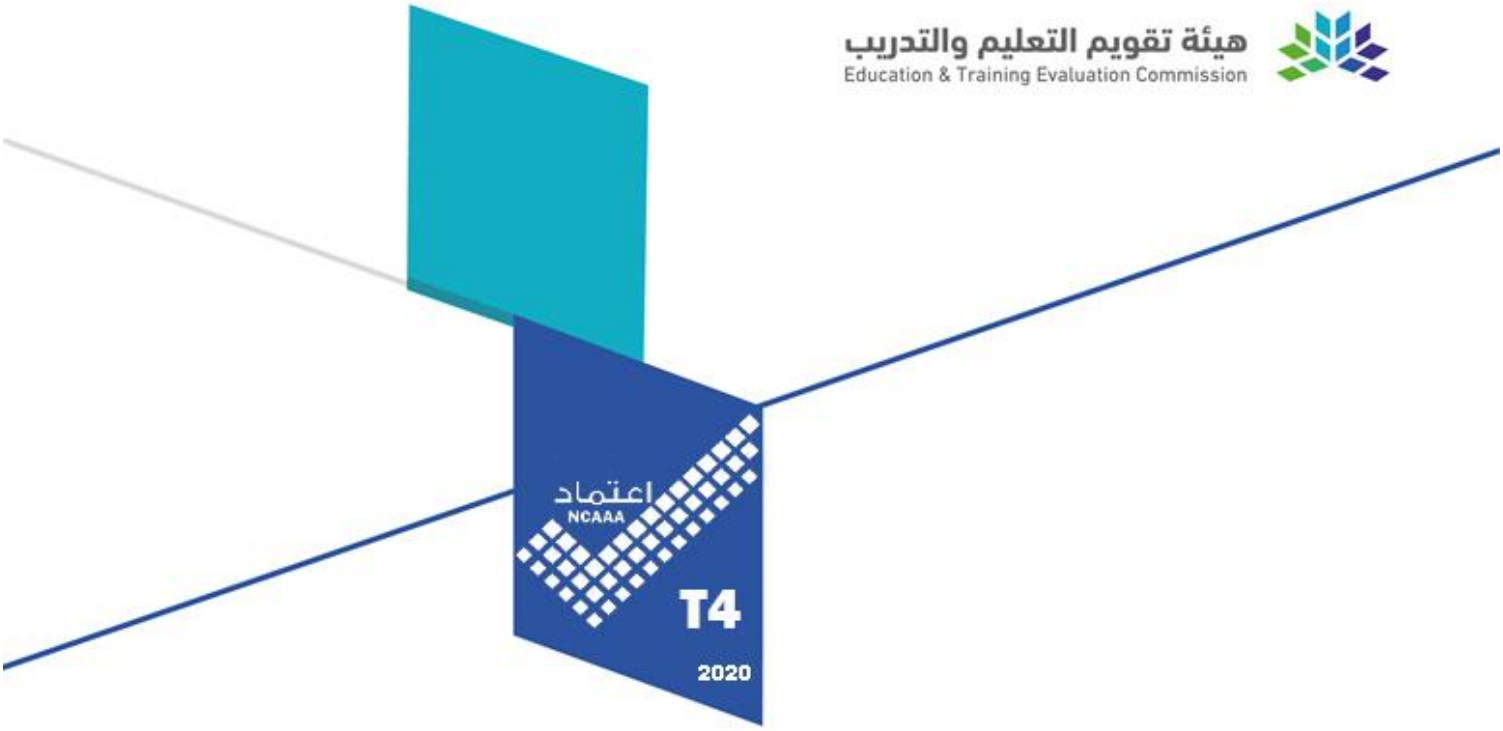
هيئة تقويم التعليم والتدريب
Education & Training Evaluation Commission



Course Specifications

Course Title:	Digital Logic
Course Code:	111 CNET – 3
Program:	Bachelor in Computer and Network Engineering Bachelor in Computer Science
Department:	Computer and Network Engineering
College:	Computer Science and Information Technology
Institution:	Jazan University

Table of Contents

A. Course Identification

1. Credit hours:	3 Hours
2. Course type	
a.	University ☐ College ☐ Department ☑ Others ☐
b.	Required ☑ Elective ☐
3. Level/year at which this course is offered:	Level 8 / Year 03
4. Pre-requisites for this course (if any)**:**	None
5. Co-requisites for this course (if any)**:**	None

6. Mode of Instruction (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	**Traditional classroom**	52	100%
2	**Blended**	--	--
3	**E-learning**	--	--
4	**Distance learning**	--	--
5	**Other**	--	--

7. Contact Hours (based on academic semester)

No	Activity	Learning Hours
Contact Hours		
1	**Lecture**	22
2	**Laboratory/Studio**	22
3	**Tutorial**	--
4	**Others** (specify)	8
	Total	52

B. Course Objectives and Learning Outcomes

1. Course Description

This course presents the various binary systems suitable for representing information in digital systems and binary codes are illustrated. It introduces the basic postulates of Boolean algebra and shows the correlation between Boolean expressions and their corresponding logic diagrams. It covers the map method for simplifying Boolean expressions. The map method is also used to simplify digital circuits constructed with AND-OR, NAND and NOR gates. The procedures to develop and conduct appropriate experimentation for the analysis and design of Combinational and Sequential circuits with Verilog. It deals with various sequential circuit components such as registers, shift registers and counters with memory circuits.

2. Course Main Objectives:

- Explain the concept of digital system with various number systems.
- Describe the Boolean expressions with Boolean Algebra Theorems.
- Simplify the map methods to reduce the Boolean Functions.
- Design of Hardware Description Languages such as Verilog.
- Design and apply the applications of Combinational and Sequential circuits.
- Analyze and design of Memory elements.

3. Course Learning Outcomes

CLOs		Aligned PLOs
1	**Knowledge and Understanding**	
1.1	**Explain** the digital system and their usage in computing engineering and latest trends.	K3
1.2	**Identify** number systems and their conversion with coding schemes.	K2
1.3	**Describe** Boolean expressions and their simplification using axiomatic properties and K-Map.	K2
2	**Skills :**	
2.1	**Design** the Boolean function from basic logic gates, universal logic gates and truth tables using latest tools.	S3
2.2	**Apply** the design of Combinational and Sequential circuit and their use in applications.	S2
2.3	**Analyze** the design with Verilog and working of Registers and their and construction using sequential circuits.	S5
3	**Values:**	
3.1	**Conduct** the projects and experiments with digital circuit kits of combinational and sequential logic and also design them with Verilog.	V1

C. Course Content

No	List of Topics	Contact Hours
1	**Chapter 1: Digital Systems and Binary Numbers** • Digital Systems • Binary Numbers • Number-Base Conversions • Octal and Hexadecimal Numbers • Complements of Numbers • Signed Binary Numbers • Binary Codes – BCD, Gray Codes and ASCII • Binary Storage and Registers • Binary Logic	4T+4P
2	**Chapter 2: Boolean Algebra and Logic Gates** • Introduction • Basic Definitions • Axiomatic Definition of Boolean Algebra • Basic Theorems and Properties of Boolean Algebra • Boolean Functions • Canonical and Standard Forms • Other Logic Operations • Digital Logic Gates	4T+4P
3	**Chapter 3: Gate Level Minimization** • Introduction • The Map Method • Four-Variable K-Map • Product-of-Sums Simplification • NAND and NOR Implementation	5T+4P

	• Exclusive-OR Function – Parity generator • Hardware Description Language – Introduction	
4	**Chapter 4: Combinational Logic** • Introduction • Combinational Circuits • Binary Adder-Subtractor • Decoders • Encoders • Multiplexers • Verilog Model	5T+6P
5	**Chapter 5: Synchronous Sequential Logic** • Introduction • Sequential Circuits • Storage Elements: Latches • Storage Elements: Flip-Flops • State Equation, State Table and State Diagram of Sequential Circuit. • Registers • Shift Registers • Ripple Counters – BCD Ripple Counter • Synchronous Counters	4T+4P
6	Final Exam	4T+4P
Total		52

Online Study Topics:
• Block diagram of Digital Computer • Integrated Circuits and Digital Logic Families • Don't care conditions – K Map • Other Two Level Implementations • Universal Shift Register

D. Teaching and Assessment

1. Alignment of Course Learning Outcomes with Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Teaching Strategies	Assessment Methods
1.0	**Knowledge and Understanding**		
1.1	**Explain** the digital system and their usage in computing science.	➢ Lectures ➢ Classroom Discussion	Midterm Exam Final Exam Assignment-1
1.2	**Identify** number systems and their conversion with coding schemes.	➢ Lectures ➢ Classroom Discussion	Midterm Exam Final Exam Assignment-1

Code	Course Learning Outcomes	Teaching Strategies	Assessment Methods
1.3	**Describe** Boolean expressions and their simplification using axiomatic properties and K-Map.	➢ Lectures ➢ Classroom Discussion	Midterm Exam Final Exam Assignment -1
2.0	**Skills**		
2.1	**Design** the Boolean function from basic logic gates, universal logic gates and truth tables.	➢ Lectures ➢ Lab ➢ Classroom Discussion	Midterm Exam Final Exam Assignment-2 Lab Exam
2.2	**Apply** the design of Combinational and Sequential circuit and their use in applications.	➢ Lectures ➢ Lab ➢ Classroom Discussion	Final Exam Assignment-2 Mini-Project Lab Exam
2.3	**Analyze** the design with Verilog and working of Registers and their and construction using sequential circuits.	➢ Lectures ➢ Classroom Discussion	Final Exam Mini-Project Assignment-2
3.0	**Values**		
3.1	**Conduct** the projects and experiments with digital circuit kits of combinational and sequential logic and also design them with Verilog.	➢ Lab Exercises	Lab Exam Mini-Project

2. Assessment Tasks for Students

#	Assessment task*	Week Due	Percentage of Total Assessment Score
1	Assignments / Mini Project	4th Week	20%
2	Midterm Exam	6th Week	20%
3	Lab Exam	11th Week	20%
4	Final Theory Exam	12th Week	40%

***Assessment task** (i.e., written test, oral test, oral presentation, group project, essay, etc.)

E. Student Academic Counseling and Support

Arrangements for availability of faculty and teaching staff for individual student consultations and academic advice :

Department have an arrangement for "Academic Counseling and Support" for each student by the department. The Department Coordinator nominates faculty members for "**Student Academic Advisory Committee"** every semester. These **"Academic Advisors"** are responsible for student counseling and advising to a group of fix number of students (around 10-15 students) and maintaining students' files. At the beginning of semester and at time of course registration all students take counseling from Academic Advisor according to his previous grades and coverage of pre-requisite course and follow-up.

In addition, students with GPA below than 2.00 are remained under deep observation and continuous meetings with respective course teachers about their performance are arranged to help and support the students. The course teacher is to be associated with this course provide a proper guidance for

students who are looking to focus on their future career based on their intellectual interests, identify better opportunities related to this course and connections in their academic fields.

F. Learning Resources and Facilities

1.Learning Resources

Required Textbooks	M. Morris Mano and Michael D. Ciletti ," Digital Design with an introduction to HDL,VHDL and System Verilog", Prentice Hall, Pearson Education International, 6th Edition, 2018. ISBN: 9780132774208
Essential References Materials	Ronald J, Tocci, Neal S. Widmer, and Gregory L. Moss, "Digital Systems: Principles and Applications", Prentice Hall, 10th edition, 2016, ISBN 0-13-111120-5.
Electronic Materials	1. JazanUniversity: http://www.jazanu.edu.sa/sites/en/Pages/Default.aspx 2. Black Board: https://lms.jazanu.edu.sa/webapps/blackboard/execute/courseMain?course_id=_26807_1&task=true&src
Other Learning Materials	----

2. Facilities Required

Item	Resources
Accommodation (Classrooms, laboratories, demonstration rooms/labs, etc.)	One lecture room equipped with projector. (maximum 30 students at a time)
Technology Resources (AV, data show, Smart Board, software, etc.)	Verilog Simulator – verilator 4.030
Other Resources (Specify, e.g. if specific laboratory equipment is required, list requirements or attach a list)	One specialized hardware lab fully equipped with various Hardware Kits Such as Trainer Kit and Experiment Module Kits with Connecting Wires accessories.

G. Course Quality Evaluation

Evaluation Areas/Issues	Evaluators	Evaluation Methods
Sufficiency of resources and facilities for students	Students	Course evaluation survey form
Effectiveness of teaching / learning process	Students	Course evaluation survey form

Evaluation Areas/Issues	Evaluators	Evaluation Methods
Effectiveness of teaching / learning process	HOD/QAU	Course reports / result analysis
Quality of learning Resources	Track leaders	Review meetings and star rating with suggestions for further modification and improvements
Verifying standards of student achievement / evaluation	HOD / committee nominated by HOD	Random re-checking of evaluated answer sheets
Achievement of course learning outcomes	Course Teachers and Course coordinators / QAU	CLO assessment template that is further verified at course coordinator, Track leader and QAU level.

Evaluation areas (e.g., Effectiveness of teaching and assessment, Extent of achievement of course learning outcomes, Quality of learning resources, etc.)
Evaluators (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify)
Assessment Methods (Direct, Indirect)

H. Specification Approval Data

Council / Committee	
Reference No.	
Date	