هيئة تقويم التعليم والتدريب
Education & Training Evaluation Commission

2023
TP-153

Course Specification
(Bachelor)

Course Title:	Computer Architecture
Course Code:	COMP 332
Program:	Bachelor in Computer Science
Department:	Computer Science
College:	College of Computer Science and Information Technology
Institution:	Jazan University
Version:	V2
Last Revision Date:	04-December-2022

Table of Contents

A. General information about the course:

1. Course Identification

1. Credit hours: (3)					
2. Course type					
A.	☐University	☐College	☒ Department	☐Track	☐Others
B.	☒ Required		☐Elective		
3. Level/year at which this course is offered: (7/3)					
4. Course general Description:					

This course is about the structure and basic function of computers. Its purpose is to present, as clearly and completely as possible, the nature and characteristics of modern-day computer systems. This course covers all aspects of computer, from the underlying integrated circuit technology used to construct computer components, to the increasing use of parallel organization concepts. This course also focuses on different elements of Computer Organization and Major components which include processor, memory, I/O, control unit, registers, ALU, and instruction execution unit. It also discusses control signals for the operation and coordination of all processor components.

5. Pre-requirements for this course (if any)**: None**

6. Pre-requirements for this course (if any)**: None**

7. Course Main Objective(s):

1. Explain the architecture and organization of computing systems
2. Describe the major components of a computer and their interconnections, both with each other and the outside world.
3. Demonstrate the program execution, instruction format and instruction cycle.
4. Illustrate various internal architectures and organizations of the processor

2. Teaching mode (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	Traditional classroom	60	100
2	E-learning		
3	Hybrid • Traditional classroom • E-learning		
4	Distance learning		

3. Contact Hours (based on the academic semester)

No	Activity	Contact Hours
1.	**Lectures**	28
2.	**Laboratory/Studio**	28
3.	**Field**	
4.	**Tutorial**	
5.	**Others (specify)**	4
Total		60

B. Course Learning Outcomes (CLOs), Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Code of CLOs aligned with program	Teaching Strategies	Assessment Methods
1.0	**Knowledge and understanding**			
1.1	**Explain** the various concepts related with the computers and machine instructions.	K1	Visual &Verbal [Lectures / Presentations]	Exam 1, Assignment(s), Final Exam
1.2	**Relate** various components, functions and interconnection structure and I/O module techniques of a computer system.	K2	Visual &Verbal [Lectures / Presentations]	Exam 1, Assignment(s), Final Exam
...				
2.0	**Skills**			

Code	Course Learning Outcomes	Code of CLOs aligned with program	Teaching Strategies	Assessment Methods
2.1	**Analyze** various memory storage and access techniques based on various performance criteria.	S1	Visual &Verbal [Lectures / Presentations]	Exam 1, Assignment(s), Final Exam
2.2	**Evaluate** the trade-offs involved in memory hierarchy design, including cache organization, virtual memory systems, and memory management techniques.	S2	Visual &Verbal [Lectures / Presentations]	Assignment(s), Final Exam
2.3…	**Design** programs based on various microprocessor concepts in Assembly language.	S3	Visual &Verbal [Lectures / Presentations]	Internal Lab Exam, Final Lab Exam
3.0	**Values, autonomy, and responsibility**			
3.1	**Demonstrate** the ability to work as a team member and take responsibility for successful completion of group assignment on recent trends of subject area.	V2	Visual &Verbal [Lectures / Presentations]	Group Assignment

C. Course Content

No	List of Topics	Contact Hours
1.	**Chapter1-Introduction: Basic Concept and Computer Evolution** • Computer, Architecture & Organization • Structure and function • Structural-Simple single- processor computer • Structure-Multicore computer • Generation of computers **(Self Study)** • Von Neumann machines/IAS • IAS Memory • Expanded Structure Of von Neumann Architecture or IAS computer • Moore's Law, Consequences of Moore's law • The Evolution of the Intel x86 Architecture	**6T + 6P**

No	List of Topics	Contact Hours
2.	**Chapter 2-A Top-Level View of Computer Function and Interconnection** • Computer components • Hardwired Program and Software • Major components • Computer Function: Instruction fetch and execute • Instruction fetch and execute • Interrupts • Multiple Interrupts • Interrupt Instruction Cycle • Interconnection Structures • Bus Interconnection **(Self Study)**	**4T + 4P**
3.	**Chapter 3 -Computer Memory System and Cache memory** • Computer Memory System Overview • Key Characteristics of Computer Memory Systems • Memory hierarchy • Cache Memory Cache Memory Principals • Cache/Main Memory Structure • Elements of cache design • Cache Address-Logical cache address or Physical cache address, • Cache Size **(Self-Study)** • Cache Memory Mapping • Replacement Algorithm.	**4T + 4P**
4.	**Chapter-4- Internal memory** • Semiconductor main memory • Main Memory Organization • Semiconductor memory types • Random Access Memory-RAM • Dynamic RAM -DRAM and Static RAM- SRAM • Read Only Memory-ROM • Types of ROM • Newer Nonvolatile Solid-State Memory Technologies **(Self Study)**	**4T + 4P**
5.	**Chapter 5-External memory** • Magnetic disc • Read and Write Mechanisms • Data organization and formatting • Constant angular velocity & multiple zone recording. • Physical Characteristics of Disk System • Disk performances parameters • Redundant Array of Independent Disks-RAID • Different RAID levels	**4T + 4P**

No	List of Topics	Contact Hours
	• RAID comparison • Solid State Drives • Optical Storage **(Self Study)** • Magnetic Tape **(Self Study)**	
6.	**Chapter 6- Input-Output** • I/O Module • External Devices/Peripheral devices • Types of External Devices **(Self Study)** • Functions of I/O module • Input-Output Technique • I/O Commands • Programmed I/O • Interrupt driven I/O • Direct memory access • DMA Operation	**4T + 4P**
7.	**Chapter 7- Instruction Sets: Characteristics and Functions** • Machine Instruction Characteristics • Elements of a Machine Instruction • Instruction Representation • Instruction Types • Instruction Set Design	**2T+2P**
8.	Lab Exam + Revision	2T + 2P
	Total	**28T+28P**

D. Students Assessment Activities

No	Assessment Activities *	Assessment timing (in week no)	Percentage of Total Assessment Score
1.	**Assignment-1**	3rd -4th week	10%
2.	**Mid Exam**	7th-8th week	15%
3.	**Assignment-2 (Group Assignment)**	9th -10th week	15%
4.	**Final Lab Exam + Lab Assignment**	As per schedule	20%
5.	**Final Theory Exam**	As per schedule	40%
	Total		100%

*Assessment Activities (i.e., Written test, oral test, oral presentation, group project, essay, etc.).

E. Learning Resources and Facilities

1. References and Learning Resources

Essential References	William Stallings, "Computer Organization and Architecture-Designing for Performance", Pearson Publication, 11th edition, 2018, ISBN-978-0134997193
Supportive References	Linda Null , Julia Lobur, "Essentials of Computer Organization and Architecture", Jones & Bartlett Learning, 5th edition, 2018, ISBN-13 : 978-1284123036
Electronic Materials	http://williamstallings.com/ComputerOrganization/
Other Learning Materials	Emulator emu8086

2. Required Facilities and equipment

Items	Resources
facilities (Classrooms, laboratories, exhibition rooms, simulation rooms, etc.)	Classroom and Lab equipped with workstation Computers and Seating Capacity for 30-40 students along with projectors.
Technology equipment (Projector, smart board, software)	The practical should be placed in a lab with the following requirements: • Computer connected to projector. • 30-40workstations • emu8086 software
Other equipment (Depending on the nature of the specialty)	

F. Assessment of Course Quality

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of teaching	Students	Indirect (Course evaluation survey form)
Effectiveness of Students assessment	CRC / QAU / HoD	Direct (Course reports / result analysis)
Quality of learning resources	Track leaders / CRC	Indirect (Review, meetings and star rating with suggestions for further modification and improvements)
The extent to which CLOs have been achieved	CRC / QAU	Direct (CLO assessment template further verified at course coordinator, Track leader and QAU level)
Other		

Assessors (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify)
Assessment Methods (Direct, Indirect)

G. Specification Approval

COUNCIL /COMMITTEE	DEPARTMENT COUNCIL
REFERENCE NO.	
DATE	15-10-2022